



High sensitive photodiodes

General Description

The epc200 is a high-sensitive, high-speed, low-cost photo diode for light-barriers, light-curtains, and similar applications. These photo diodes are designed to be used in a reverse-bias mode, whereas the reverse bias voltage can be between 1.5 and 20 Volts. This device allows the design of short to long range light barriers from a few millimeters up to tens of meters.

The diodes feature a very high quantum efficiency of 90% in the near IR range, a reverse breakdown voltage of up to 30 Volts and a response time down to less than 100ns.

The advanced Chips Scale Package (CSP) makes this device ideal for miniaturized systems where a minimal space requirement is key.

Features

- Low dark current
- High sensitivity
- High dynamic range
- CSP package with very small footprint
- Customer specific wavelength filter on request
- Fully standard SMD assembly process compatible

Applications

- Light barriers and light curtains
- Light barriers ranging from millimeters to tens of meters
- Light curtains
- Smoke detectors
- Liquid detectors
- Heart beat monitors
- Oximeters
- Position detection (rotary, linear, angle, etc.)
- IR remote control of Hi-Fi, TV sets and other equipment

Product image

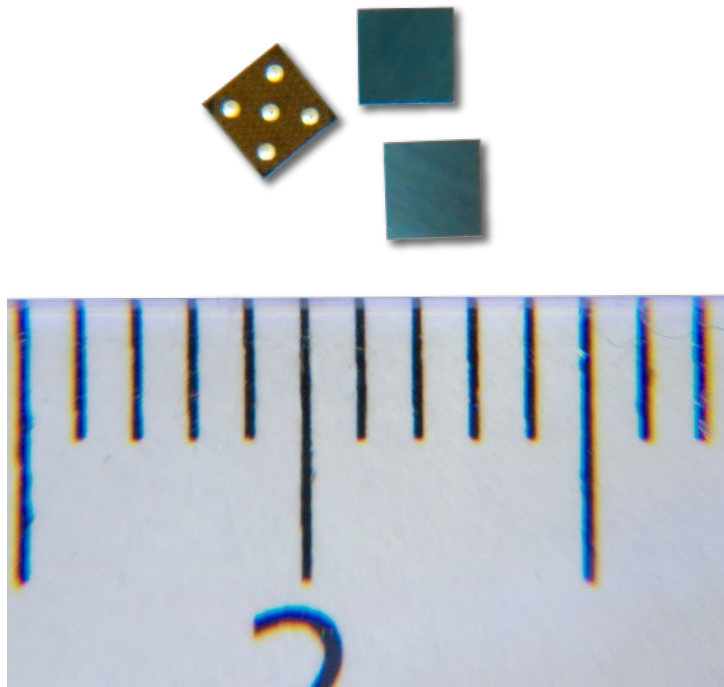


Figure 1: epc200 photo diodes

Absolute Maximum Ratings (Notes 1, 2)		Recommended Operating Conditions			
Reverse Voltage V_R	30.0 V	Reverse Voltage (V_R)	Min. 1.5	Max. 20.0	Units V
Storage Temperature Range (T_s)	-40°C to +85°C	Operating Temperature (T_A)	-40	+85	°C
Lead Temperature solder, 4 sec. (T_L)	+260°C	Relative Humidity (non-condensing)	+5	+95	%
Expected Lifetime (MTBF)	500 * 10 ⁶ h @ 25°C (<2 FIT)				

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical Characteristics.

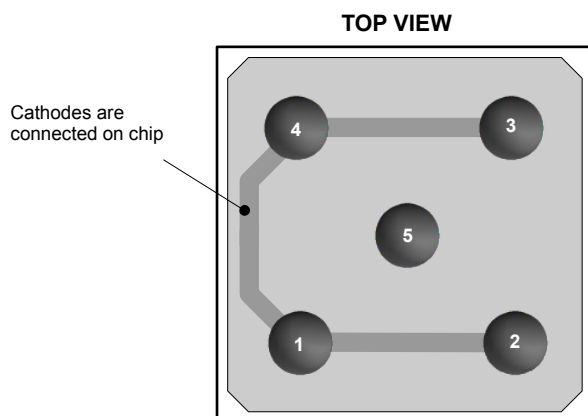
Note 2: This device is a highly sensitive CMOS photodiodes with an ESD rating of JEDEC HBM class 2 (2kV to <4kV). Handling and assembly of this device should only be done at ESD protected workstations.

General Characteristics

Unless otherwise stated, measuring parameters are $V_R = 5.0$ V, $-40^\circ\text{C} < T_A < +85^\circ\text{C}$, $R_L = 50 \Omega$

Symbol	Parameter	Conditions/Comments	Values			Units
			Min.	Typ.	Max.	
$\lambda_{S \text{ max.}}$	Wavelength	max. Sensitivity		850		nm
λ	Wavelength Range	$S = 20\%$ of S_{max}	450		1050	nm
S_A	Spectral Sensitivity	$\lambda = 850\text{nm}$, $V_R = 5\text{V}$, $I_e = 1 \text{ mW/cm}^2$ $\lambda = 950\text{nm}$, $V_R = 5\text{V}$, $I_e = 1 \text{ mW/cm}^2$		0.61 0.43		A/W A/W
η	Quantum Efficiency	$\lambda = 850\text{nm}$, $V_R = 5\text{V}$, $I_e = 1 \text{ mW/cm}^2$ $\lambda = 950\text{nm}$, $V_R = 5\text{V}$, $I_e = 1 \text{ mW/cm}^2$		90 62		%
ϕ	Half angle			± 60		°
V_O	Open Circuit Voltage	$I_e = 0.5 \text{ mW/cm}^2$		250		mV
TC_V	Temperature Coefficient of I_{SC}			0.25		%/K
TC_O	Temperature Coefficient of V_O			-3.0		mV/K
I_P	Photo Current	$V_R = 5\text{V}$, $I_e = 1 \text{ mW/cm}^2$, $\lambda = 850 \text{ nm}$ $V_R = 5\text{V}$, $I_e = 1 \text{ mW/cm}^2$, $\lambda = 950 \text{ nm}$		18.7 13.2		μA
I_R	Dark Current	$V_R = 5 \text{ V}$, $T_A = 20^\circ\text{C}$ $V_R = 20 \text{ V}$, $T_A = 20^\circ\text{C}$ Selected types with reduced dark current on request		2 5	20	nA
I_{SC}	Short-circuit Current	$I_e = 1 \text{ mW/cm}^2$, $\lambda = 850 \text{ nm}$		20		μA
t_r	Rise/Fall Time	$V_R = +1.5 \text{ V}$ $V_R = +5.0 \text{ V}$ $V_R = +10.0 \text{ V}$	photo current measured at $R_L = 50 \Omega$, $\lambda = 850 \text{ nm}$, $I_P = 200 \mu\text{A}$			ns
C_O	Capacitance	$V_R = +5\text{V}$, $f = 100\text{kHz}$, $E = 0$		22		pF
NEP	Noise Equivalent Power	$V_R = 5 \text{ V}$			1.2×10^{-14}	W/ $\sqrt{\text{Hz}}$

Connection Diagram

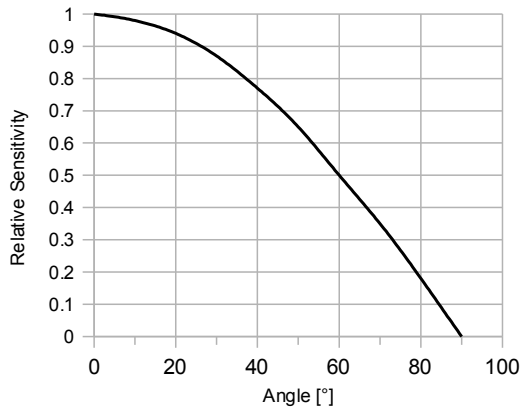


Pin	Assignment
1	Cathode
2	Cathode
3	Cathode
4	Cathode
5	Anode

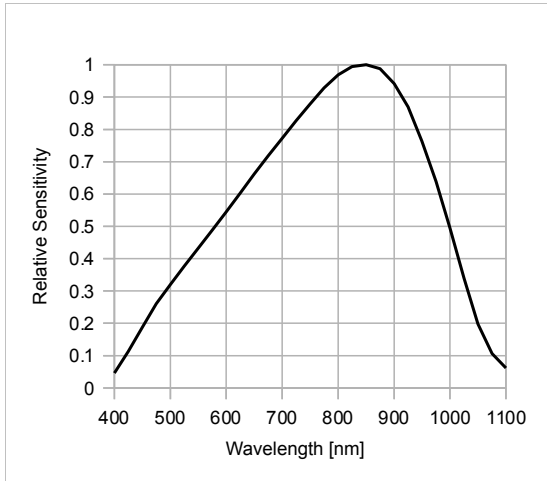
Figure 2: Chip connections

Other Parameters

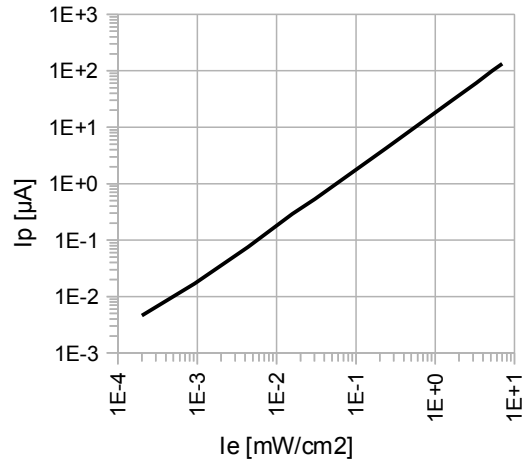
(typical values, $T_{amb} = 25^{\circ}\text{C}$, $V_{DD} = 5.0\text{V}$, $I_{PD}=0\text{mA}$)



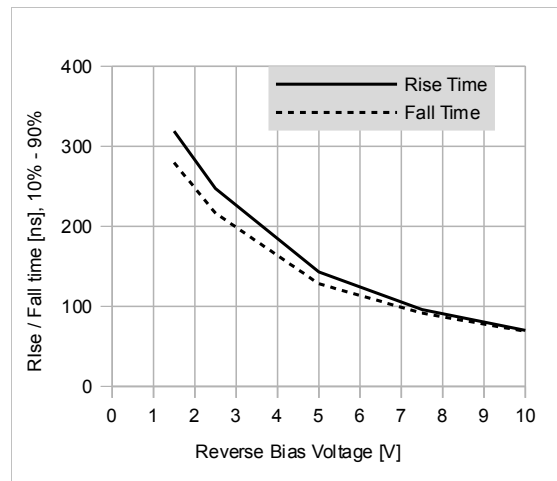
Relative sensitivity vs. illumination angle



Relative spectral sensitivity (no daylight filter)



Photocurrent $I_P = f(I_e)$, $V_R = 5\text{V}$, $\lambda = 850\text{nm}$



Rise / fall time versus reverse bias voltage

Application Information

A typical application of this chip is shown in Figure 3. In this application, a reverse bias voltage of approx. 1.5 V is used. Since the applications are typically light barriers as shown in Figure 1, dark current is not important at all, even in the range of up to 100nA.

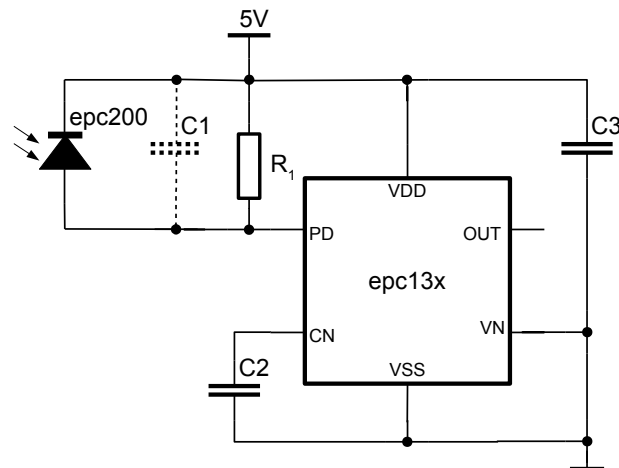


Figure 3: Typical schematic circuit using an epc13x photo pulse amplifier

Recommended Components Values (examples only – depends on particular application case)

R1: 27k (bias resistor). Sensitivity can be reduced by the reduction of this resistor.

C1: Usually not needed. May be up to 100 pF (refer to the epc13x data sheet).

C2: 33nF (DC input current filter capacitor)

C3: 100nF or more (power supply filter capacitor)

Spectral Sensitivity

This photo diode contains an anti-reflection coating on the photosensitive surface. Standard versions have no optical filter in order to allow applications from the near UV to the near IR range. However, optical filters deposited on the photosensitive surface are available upon request. The filter parameters can be adjusted in a wide range according to specific customer requirements.

Design rules

The cathode pins are connected on chip. A proper design ensures that all cathode pins are connected to the same voltage level. All pins of the diode array should be connected.

Layout Information (all measures in mm, \odot)

CSP5 Package

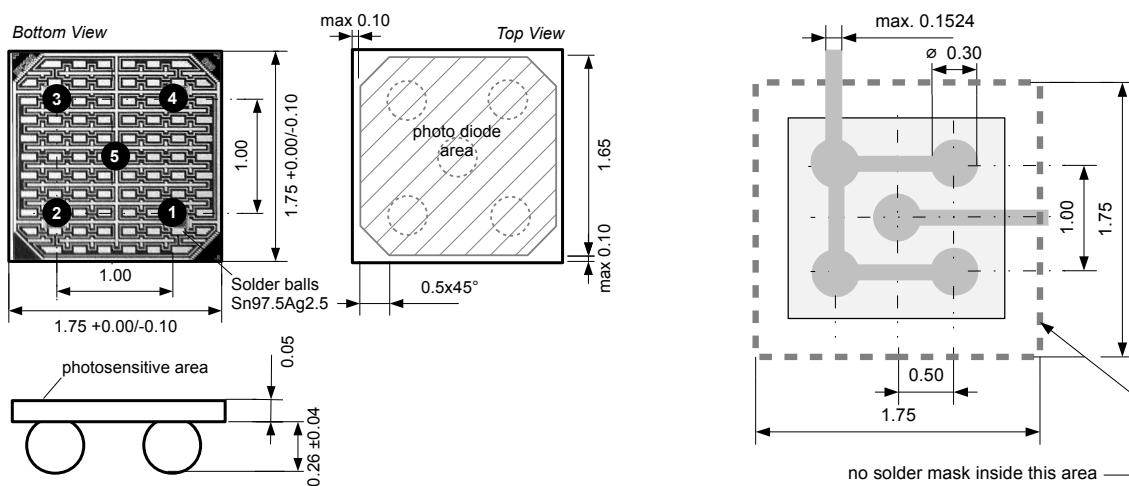


Figure 4: Mechanical dimensions

Figure 5: Layout recommendation

Packaging Information

(all measures in mm)

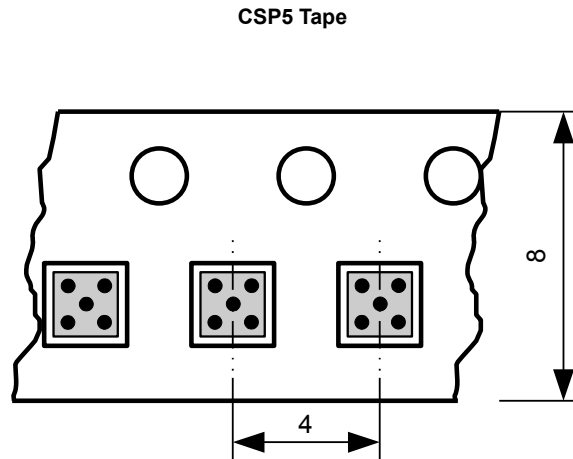


Figure 6: Carrier tape dimensions & chip orientation

Tape & Reel Information

The devices are mounted on embossed tape for automatic placement systems. The tape is wound on 330 mm (13 inch) reels and individually packaged for shipment. General tape-and-reel specification data are available in a separate data sheet and indicate the tape sizes for various package types. Further tape-and-reel specifications can be found in the Electronic Industries Association (EIA) standard 481-1, 481-2, 481-3.

epc does not guarantee non-empty cavities. Thus, pick-and-place machines should check the presence of a chip during picking.

It is highly recommended to use underfill after assembly of the chips to the PCB.

Ordering Information

Part Name	Part Number	Package	RoHS compliance	Packaging Method
epc200-CSP5	P100 179	CSP5	Yes	Reel
epc200 Chip Carrier	P100 205	PCB	Yes	Tray Tape on request

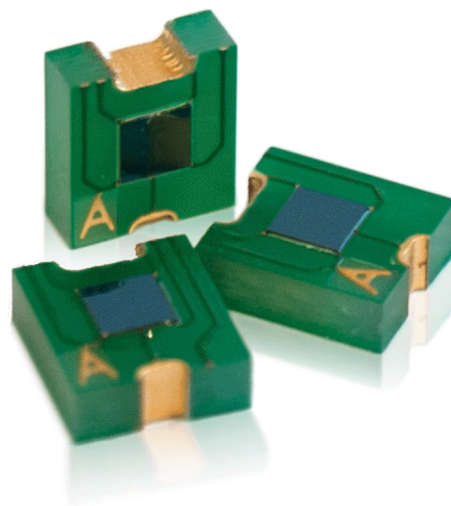


Figure 7: epc200 photo diodes on chip carrier

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